REMARKS

Upon entry of this Amendment, claims 29-48 are pending. Claims 29, 38, 39 and 48 are amended.

In the April 28, 2006 Office Action, the examiner:

- rejected claims 29, 30, 32-40 and 42-48 under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over, U.S. Patent Application Publication No. 2002/0033504 to Ohnakado ("the Ohnakado publication");
- rejected claims 29-48 under 35 U.S.C. § 103(a) as unpatentable over the Ohnakado publication in view of U.S. Patent No. 5,741,740 to Jang ("the Jang patent");
- rejected claims 29, 30, 32-40 and 42-48 under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. § 103(a), as obvious over, U.S. Patent No. 5,674,761 to Chang et al. ("the Chang patent"); and
- rejected claims 29-48 under 35 U.S.C. § 103(a) as unpatentable over the Ohnakado publication in view of the Jang patent, and further in view of U.S. Patent No. 4,646,427 to Doyle ("the Doyle patent").

Rejections

I. Claims 29, 30, 32-40 and 42-48 stand under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over, the Ohnakado publication

Claim 29 has been amended to recite, *inter alia*:

> ". . . first and second power supply voltage sources . . .
> a plurality of serially connected polycrystalline silicon diodes . . . each diode having a first portion . . . and a second portion . . . the first and second portions being adjoined to form an electrical junction;
> wherein the second portion of one of the plurality of diodes is connected to the first portion of a subsequent one of the plurality of diodes; and
> wherein a first diode of the plurality of diodes has its first portion connected to the first power supply voltage source, and a last diode of the plurality of diodes has its second portion connected to the second power supply voltage source."

Claim 39 has been amended to recite, *inter alia*,

> ". . . first and second power supply voltage sources;
> a first power distribution network connected to the first power supply voltage source;
> a second power distribution network connected to the second power supply voltage source;
> an internal circuit connected between the first and second power distribution networks; and
> an electrostatic discharge circuit connected between the first power supply voltage source and the second power supply voltage source . . . said electrostatic discharge circuit comprising . . .
> a plurality of serially connected polycrystalline silicon diodes."

The Ohnakado publication does not anticipate claim 29 or 39, because it fails to disclose, either expressly or inherently, every limitation of those claims. Specifically, the Ohnakado application fails to disclose ". . . first and second power supply voltage sources . . . a plurality of serially connected polycrystalline silicon diodes . . . wherein the second portion of one of the plurality of diodes is connected to the first portion of a subsequent one of the plurality of diodes; and wherein a first diode of the plurality of diodes has its first portion connected to the first power supply voltage source, and a last diode of the plurality of diodes has its second portion connected to the second power supply voltage source," as required by claim 29; or "first and second power supply voltage sources; a first power distribution network connected to the first power supply voltage source; a second power distribution network connected to the second power supply voltage source . . . an electrostatic discharge circuit connected between the first power supply voltage source and the second power supply voltage source . . . said electrostatic discharge circuit comprising . . . a plurality of serially connected polycrystalline silicon diodes," as required by claim 39.

Rather, the Ohnakado publication discloses a plurality of diodes 38a-m connected between a high frequency I/O signal line which connects high-frequency signal I/O pad 30a with internal circuit 100 and VDD (positive voltage supplied externally). (*See* the Ohnakado publication, paragraph [00070] and Fig. 10.) A plurality of diodes 39a-n are connected in series between the ground (GND) and the high-frequency I/O signal line. (*See id.*) Thus, although the Ohnakado publication discloses a plurality of diodes used for ESD protection between the

external contacts (I/O pads) of the device, it fails to disclose their use in the structural combination claimed in independent claims 29 and 39, namely "a first diode of the plurality of diodes [having] its first portion connected to the first power supply voltage source, and a last diode of the plurality of diodes [having] its second portion connected to the second power supply voltage source," as required by claim 29; or "a first power distribution network connected to the first power supply voltage source; a second power distribution network connected to the second power supply voltage source . . . an electrostatic discharge circuit connected between the first power supply voltage source and the second power supply voltage source," as required by claim 39. In addition, and for the same reasons as stated regarding the non-anticipation of claims 29 and 39 by the Ohnakado publication, the Ohnakado publication fails to teach or suggest all of the elements of claims 29 and 39, as required by 35 U.S.C. § 103(a).

Thus, applicant requests that the 35 U.S.C. §§102(e) and 103(a) rejections of claims 29 and 39 be withdrawn, and that these claims be allowed. With respect to claims 30, 32-38; 40 and 42-48, which depend from independent claims 29 and 39, respectively, and recite additional features of the invention, applicant requests that the 35 U.S.C. §§102(e) and 103(a) rejections of these claims be withdrawn for the same reasons as stated for claims 29 and 39, and that these claims likewise be allowed.

II. Claims 29-48 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the Ohnakado publication in view of the Jang patent

Claism 29-48 are allowable because the Ohnakado publication and the Jang patent, taken alone or in combination, fail to disclose, teach or suggest all of the limitations of those claims. As explained in Section I above, the Ohnakado publication fails to disclose "a first diode of the plurality of diodes [having] its first portion connected to the first power supply voltage source, and a last diode of the plurality of diodes [having] its second portion connected to the second power supply voltage source," as required by claim 29; or "a first power distribution network connected to the first power supply voltage source; a second power distribution network connected to the second power supply voltage source . . . an electrostatic discharge circuit connected between the first power supply voltage source and the second power supply voltage source," as required by claim 39.

The Jang patent fails to remedy these deficiencies in the Ohnakado publication, because the Jang patent merely discloses a method for forming trench fill layers for integrated circuit fabrication. (*See* the Jang patent, col. 1, lines 7-9.) Thus, because the Ohanakdo publication and Jang patent, taken alone or in combination, fail to disclose, teach or suggest all of the limitations of claims 29-38, applicant requests that the 35 U.S.C. § 103(a) rejections of claims 29-38 be withdrawn, and that the claims be allowed.

III. Claims 29, 30, 32-40 and 42-48 stand rejected under 35 U.S.C. § 102(e) as anticipated by, or in the alternative, under 35 U.S.C. § 103(a), as obvious over, the Chang patent

The Chang patent does not anticipate independent claim 29 or 39, because it fails to disclose, either expressly or inherently, all of the limitations of those claims. The examiner states that "Chang's polysilicon 'diode' device anticipates or at least makes the claim structure [obvious] depending on one's interpretation of 'serially connected.'" (*See* Office Action, 4/28/06, pg. 4, lines 4-6.) However, the examiner provides no such "interpretation" in making this rejection.

Claims 29 and 39 make it clear what is meant by "serially connected" - specifically that ". . . the second portion of one of the plurality of diodes is connected to the first portion of a subsequent one of the plurality of diodes," as recited in claim 29; and ". . . the second portion of one of the plurality of diodes is connected to the first portion of a subsequent one of the plurality of diodes," as recited in claim 39. The Chang patent fails to disclose such an arrangement, nor does it teach or suggest the possibility or desirability of such an arrangement. Rather, the Chang patent simply discloses the use of a diode for ESD protection of an output pad 26. (*See* the Chang patent, col. 5, lines 4-17 and Fig. 9.)

Moreover, the Chang patent fails to disclose "a first diode of the plurality of diodes [having] its first portion connected to the first power supply voltage source, and a last diode of the plurality of diodes [having] its second portion connected to the second power supply voltage source," as required by claim 29; or "a first power distribution network connected to the first power supply voltage source; a second power distribution network connected to the second power supply voltage source . . . an electrostatic discharge circuit connected between the first

power supply voltage source and the second power supply voltage source," as required by claim 39. Similar to the Ohnakado arrangement, the Chang patent simply discloses the use of a diode for ESD protection of an output pad 26. (*See* the Chang patent, col. 5, lines 4-17 and Fig. 9.)

In addition, and for the same reasons as stated regarding the non-anticipation of claims 29 and 39 by the Chang patent, the Chang patent fails to teach or suggest all of the elements of claims 29 and 39, as required by 35 U.S.C. § 103(a).

Applicant therefore requests that the 35 U.S.C. §§ 102(e) and 103(a) rejections of claims 29 and 39 be withdrawn, and that these claims be allowed. With respect to claims 30, 32-38; 40 and 42-48, which depend from independent claims 29 and 39, respectively, and recite additional features of the invention, applicant requests that the 35 U.S.C. §§ 102(e) and 103(a) rejections of these claims be withdrawn for the same reasons as stated for claims 29 and 39, and that these claims likewise be allowed.

IV. Claims 29-48 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the Ohnakado publication in view of the Jang patent, and further in view of the Doyle patent

As stated in Section I above, the Ohnakado publication and Jang patent, taken alone or in combination, fail to disclose "a first diode of the plurality of diodes [having] its first portion connected to the first power supply voltage source, and a last diode of the plurality of diodes [having] its second portion connected to the second power supply voltage source," as required by claim 29; or "a first power distribution network connected to the first power supply voltage source; a second power distribution network connected to the second power supply voltage source . . . an electrostatic discharge circuit connected between the first power supply voltage source and the second power supply voltage source," as required by claim 39

The Doyle patent fails to remedy these deficiencies in the Ohnakado publication and Jang patent, because it merely discloses a method of electrostatically altering the characteristics of a polysilicon zener diode (adjusting the zener "knee"). Thus, applicant requests that the 35 U.S.C. § 103(a) rejections of claims 29-48 be withdrawn, and that these claims be allowed.

V. Dependent Claims 38 and 48

The examiner has rejected dependent claims 38 and 48 under 35 U.S.C. §§ 102(e) and 103(a), citing the Ohnakado publication, the Chang patent, and combinations thereof with the Jang and Doyle patents. Claims 38 and 48 depend from independent claims 29 and 39, respectively, and additionally recite:

> ". . . the plurality of serially connected polycrystalline silicon diodes compris[ing] "n" diodes, and the number "n" is determined by the formula:
>
> $n >= (Vnoise + |Vx1-Vx2|)/ V_T$
>
> where:
>
> n is the number of serially connected polycrystalline silicon diodes,
>
> V_{noise} is the maximum voltage level difference allowed to be present on the internal integrated circuit located between the first power supply voltage source and the second power supply voltage source,
>
> Vx1 is the magnitude of the first power supply voltage source,
>
> Vx2 is the magnitude of the second power supply voltage source, and
>
> V_T is the threshold voltage of each of the polycrystalline silicon diodes."

In explaining his anticipation rejections of these claims, the examiner stated:

> "the diodes of '504 [the Ohnakado publication] function in the same manner. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim."

(*See* Office Action mailed 4/28/06, pg. 3, lines 6-10.)

But contrary to the examiner's assertion, the limitations recited above are not merely an "intended use" of the claimed invention, but rather, they recite specific structures and properties of the elements of the claimed device. Indeed, they recite a *structural difference* between the claimed invention and the prior art. Specifically, V_{noise}, Vx1, Vx2 and V_T all are *physical characteristics* of the recited components of the device, and thus can not be rejected as merely "intended use." None of the references cited by the examiner in rejecting claims 38 and 48

disclose, teach or suggest the structural arrangement of diodes in the manner described by the formula of claims 38 and 48.

Thus, claims 38 and 48 are believed to be allowable over the cited references for these additional reasons.

Applicants submit that this application is in condition for allowance. Early notification to that effect is respectfully requested. If a telephone conference would be of assistance in advancing prosecution of the above-captioned application, the examiner is invited to call the undersigned attorney at (609) 631-2491.

No fee is believed due with this submission, however, should any fees be required, the Commissioner for Patents is hereby authorized to charge any such required fees to deposit account **04-1679.**

Respectfully submitted,

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